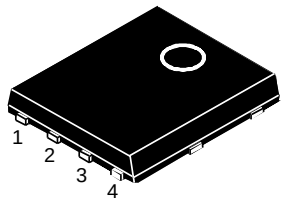
STL42P6LLF6

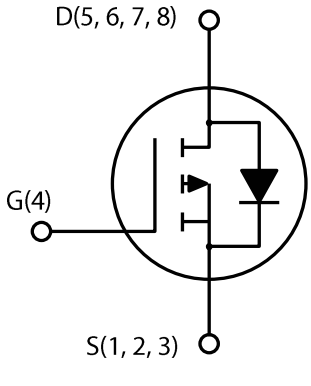
P-channel 60 V, 0.02 Ω typ., 42 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - preliminary data



PowerFLAT™5x6

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$max.	I_D
STL42P6LLF6	60 V	0.028 Ω @ 10 V	42 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits a very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL42P6LLF6	42P6LLF6	PowerFLAT ™ 5x6	Tape and reel

For the P-channel Power MOSFET, actual polarity of voltages and current have to be reversed.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C= 25 °C	42	A
I_D (1)	Drain current (continuous) at T_C= 100 °C	30	A
I_D (1)(2)	Drain current (pulsed)	168	A
I_D (3)	Drain current (continuous) at T_{pcb}= 25 °C	9	A
I_D (3)	Drain current (continuous) at T_{pcb}= 100 °C	3.3	A
I_{DM} (3)(2)	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at T_C= 25 °C	100	W
P_{TOT}	Total dissipation at T_{pcb}= 25 °C	4.8	W
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

Notes:

(1)The value is according to $R_{thj\text{-}case}$.

(2)Pulse width is limited by safe operating area.

(3)The value is according to $R_{thj\text{-}pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	1.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max.	31.3	°C/W

Notes:

(1)When mounted on FR-4 board of 15 mm ^{2}, 2 Oz Cu, t <10 sec.

For the P-channel Power MOSFET, actual polarity of voltages and current have to be reversed.

2 Electrical characteristics

(T_{case}= 25 °C unless otherwise specified).

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS}= 0, V_{DS} = 60 V			1	µA
		V_{GS}= 0, V_{DS}= 60 V, T_C =125 °C			10	µA
I_{GSS}	Gate-body leakage current	V_{DS}= 0, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 4.5 A		0.02	0.028	Ω
		V_{GS} = 4.5 V, I_D= 4.5 A		0.035	0.045	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 48 V, f = 1 MHz, V_{GS}= 0	-	1720	-	pF
C_{oss}	Output capacitance		-	220	-	pF
C_{rss}	Reverse transfer capacitance		-	106	-	pF
Q_g	Total gate charge	V_{DD}= 48 V, I_D= 9 A, V_{GS}= 4.5 V (see *Figure 3*)	-	30	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 48 V, I_D = 4.5 A, R_G= 4.7 Ω, V_{GS} = 10 V (see *Figure 2*)	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

For the P-channel Power MOSFET, actual polarity of voltages and current have to be reversed.

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		42	A
I_{SDM}	Source-drain current (pulsed)		-		168	A
V_{SD}(2)	Forward on voltage	V_{GS}= 0, I_{SD}= 4.5 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD}= 9 A, di/dt = 100 A/µs V_{DD}= 16 V, T_j = 150 °C (see *Figura 4*)	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulse duration = 300 µs, duty cycle 1.5%.

For the P-channel Power MOSFET, actual polarity of voltages and current have to be reversed.

3 Test circuits

Figure 2: Switching times test circuit for resistive load

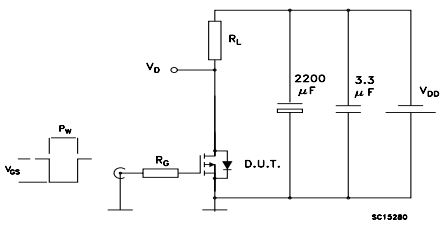


Figure 3: Gate charge test circuit

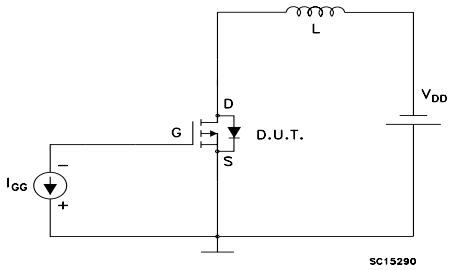
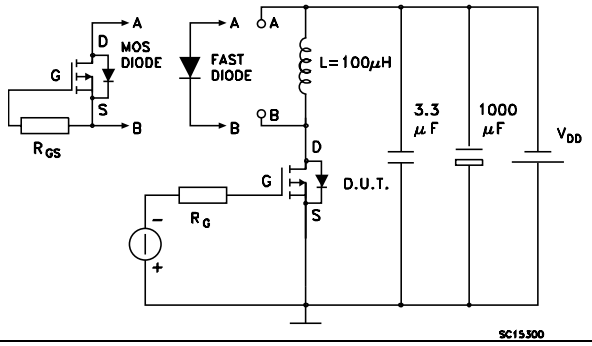


Figure 4: Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK ®packages, depending on their level of environmental compliance. ECOPACK ®specifications, grade definitions and product status are available at: www.st.com. ECOPACK ®is an ST trademark.

4.1 PowerFLAT 5x6 type S-R mechanical data and footprint

Figure 5: PowerFLAT™ 5x6 type S-R package outline

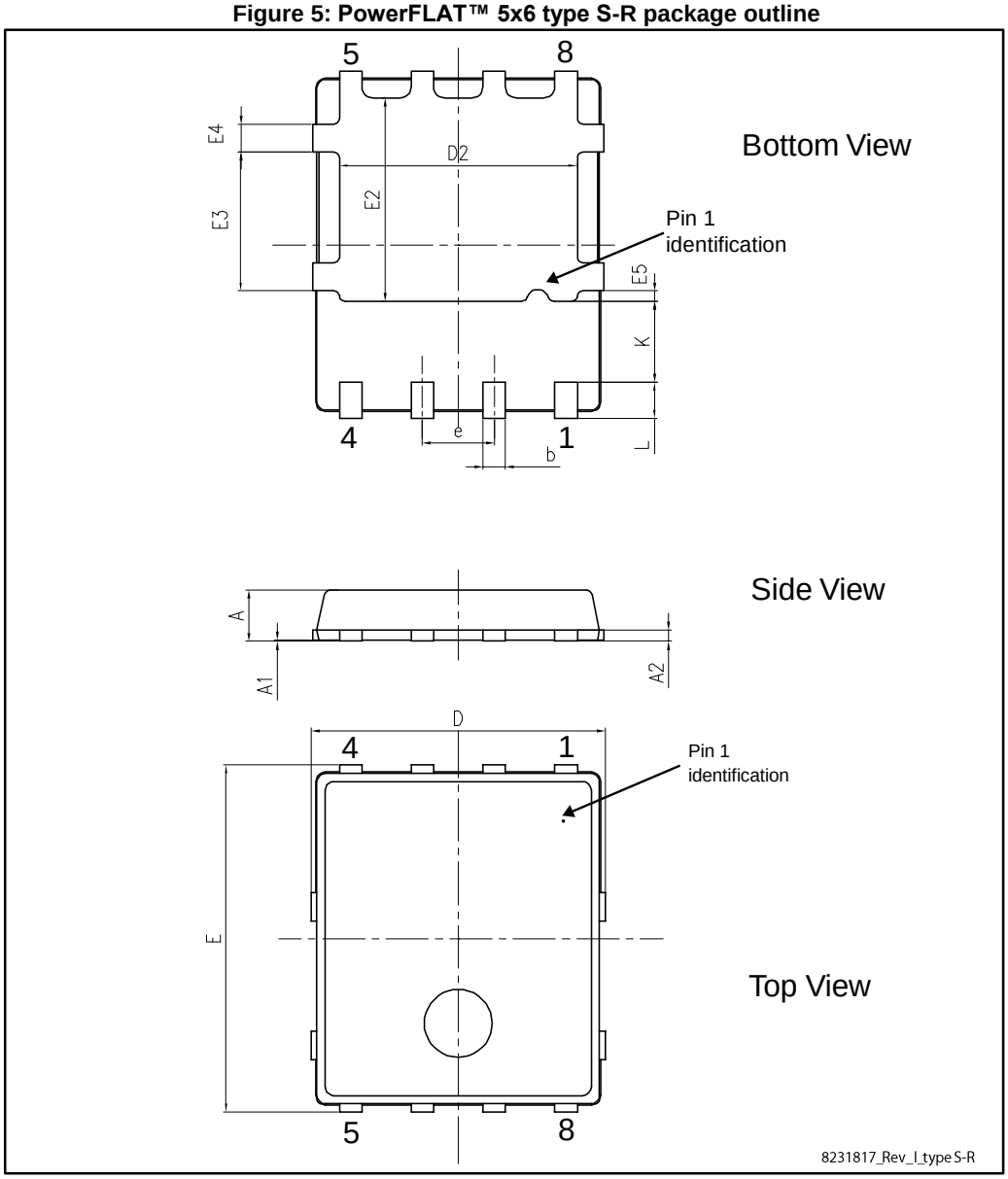
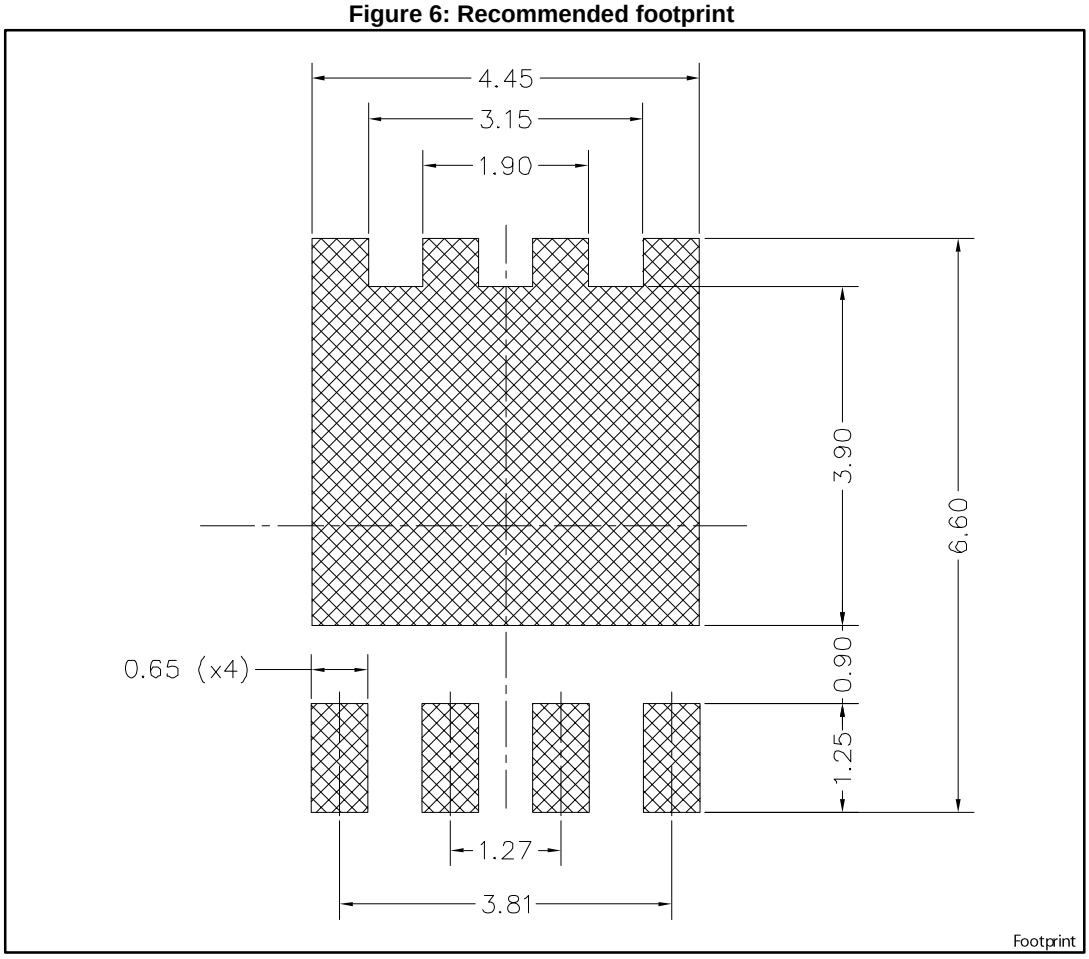


Table 8: PowerFLAT™ 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
D2	4.11		4.31
E	5.95	6.15	6.35
e		1.27	
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
K	1.275		1.575
L	0.60		0.80

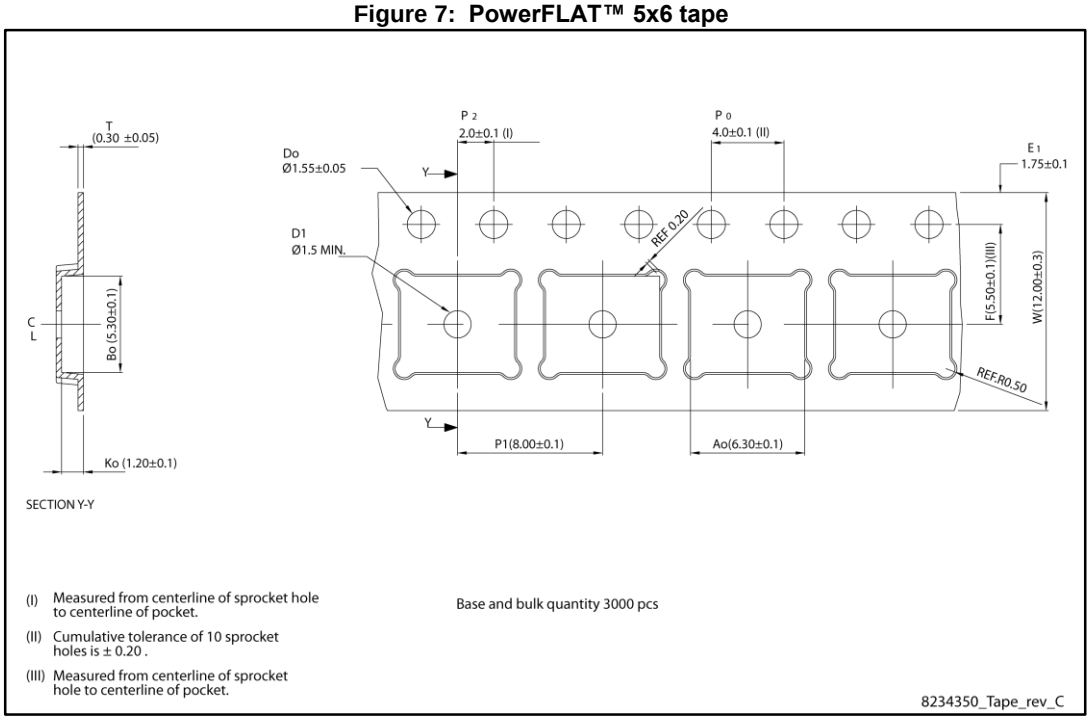
Figure 6: Recommended footprint



All dimensions are in mm.

4.2 Packaging PowerFLAT™ 5x6 tape and reel

Figure 7: PowerFLAT™ 5x6 tape



All dimensions are in millimeters.

Figure 8: PowerFLAT™ 5x6 package orientation in carrier tape

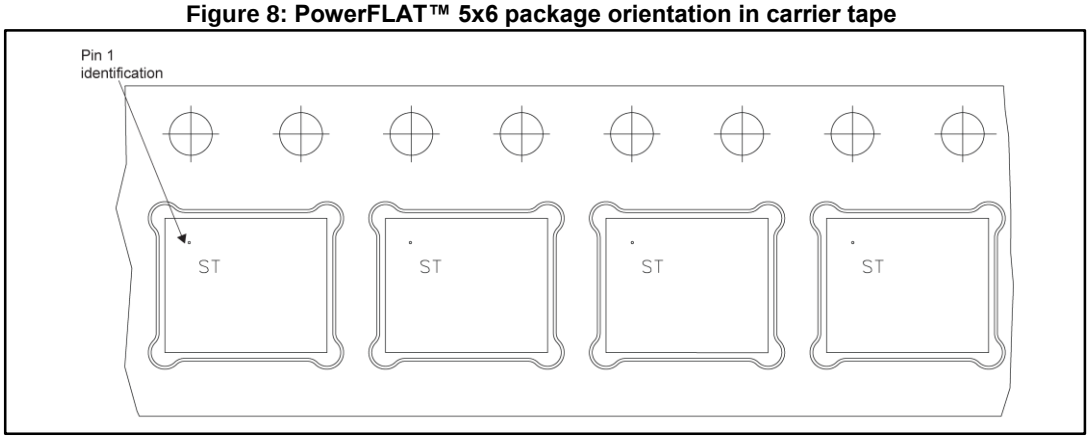
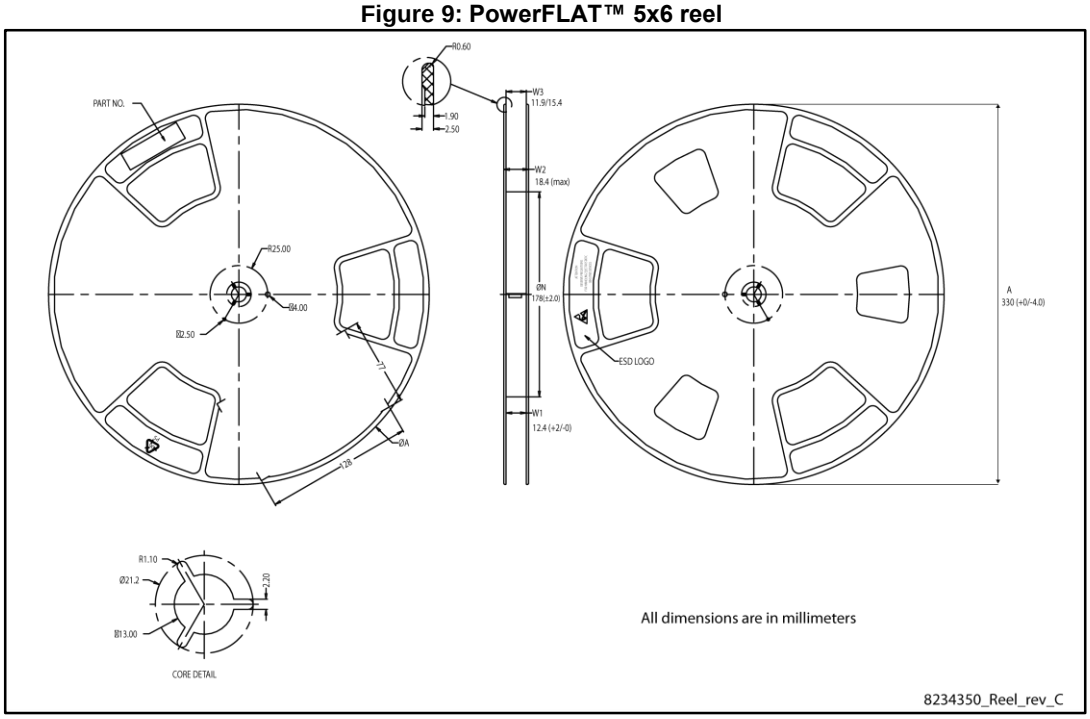


Figure 9: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Oct-2013	1	First release.
25-Aug-2014	2	Modified: *Figure 1: "Internal schematic diagram"* Updated: *Section 10: "Package mechanical data"* Minor text changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.